MECHANISM FOR SUPPORTING SELF-MODIFYING CODE IN A HARVARD ARCHITECTURE DIGITAL SIGNAL PROCESSOR AND METHOD OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

For use in a processor having separate instruction and data buses, separate instruction and data memories and separate instruction and data units, a mechanism for, and method of, supporting self-modifying code and a digital signal processor incorporating the mechanism or the method. In one embodiment, the mechanism includes: (1) a crosstie bus coupling the instruction bus and the data unit and (2) a request arbiter, coupled between the instruction and data units, that arbitrates requests therefrom for access to the instruction memory.